and etched. In step **528**, metallization is performed to from the contacts. In step **530**, the metal interconnect **324** is formed.

[**0029**] Applications for the combination of metal gate conductor with self-aligned contact structure include dynamic random access memory (DRAM), static random access memory (SRAM), non-volatile memory cells, and volatile memory cells. Within these integrated circuits (ICs), a metal gate conductor on gate dielectric on semiconductor substrate generates a MOS transistor. This can be constructed as NMOS, PMOS, CMOS, SOI NMOS, SOI PMOS, SOI CMOS, NMOS FinFET, PMOS FinFET, CMOS FinFET, or a combination of two or more.

[**0030**] The above illustration provides many different embodiments or embodiments for implementing different features of the invention. Specific embodiments of components and processes are described to help clarify the invention. These are, of course, merely embodiments and are not intended to limit the invention from that described in the claims.

[**0031**] Although the invention is illustrated and described herein as embodied in one or more specific examples, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims. Accordingly, it is appropriate that the appended claims be construed broadly and in a manner consistent with the scope of the invention, as set forth in the following claims.

**1**. A MOS device, comprising:

a gate dielectric layer disposed on a semiconductor substrate;

a metal gate conductor disposed directly on the gate dielectric layer;

a cap layer disposed on the metal gate conductor and including opposed overhang portions extending laterally beyond respective sidewalls of the metal gate conductor;

one or more spacers laterally spaced from the sidewalls of the metal gate conductor defining air voids beneath the overhang portions, the spacers contacting the cap layer, such that the cap layer and the spacers enclose the metal gate conductor therein; and

at least one self-aligned contact structure formed next to at least one of the spacers, to be in contact with the semiconductor substrate,

wherein the cap layer and the spacers separate the self-aligned contact structure from directly contacting the metal gate conductor.

**2**. The MOS device of claim 1 wherein the gate dielectric layer is made of a material including Si3N4, nitrided oxide, Hf oxide, Al2O5, Ta2O5, metal oxide, or high K dielectric constant materials (K>5).

**3**. The MOS device of claim 1 wherein the metal gate conductor has a thickness between 100 and 3,000 Angstroms.

**4**. The MOS device of claim 1 wherein the metal gate conductor is made of a material including refractory metal, nitrided metal, or silicide.

**5**. The MOS device of claim 4 wherein the metal gate conductor is made of a material including W, Al, AlCu, Cu, Ti, $TiSi_2$, Co, $CoSi_2$, Ni, NiSi, TiN, TiW, or TaN.

**6**. The MOS device of claim 1 wherein the cap layer has a thickness between 50 and 3,000 Angstroms.

**7**. The MOS device of claim 1 wherein the cap layer comprises at least a first cap sub-layer and a second cap sub-layer disposed thereupon.

**8**. The MOS device of claim 7 wherein the first cap sub-layer has a thickness between 50 and 3,000 Angstroms.

**9**. The MOS device of claim 8 wherein the second cap sub-layer has a thickness between 50 and 2,000 Angstroms.

**10**. The MOS device of claim 7 wherein the first cap sub-layer is an oxide layer and the second cap cub-layer is a nitride layer.

**11**. The MOS device of claim 1 wherein the self-aligned contact structure covers at least a portion of the cap layer.

**12**. (canceled)

**13**. (canceled)

**14**. A method for forming a gate structure for MOS devices, comprising:

depositing a gate dielectric layer on a substrate;

depositing a gate metal layer atop the gate dielectric layer;

depositing a cap layer atop the gate metal layer;

patterning the cap layer, the gate metal layer and the gate dielectric layer to form a caped gate conductor;

forming one or more spacers covering sidewalls of the caped gate conductor, including a stack of the patterned cap layer and gate metal layer;

forming an inter-level dielectric layer over the caped gate conductor, the spacers and the substrate;

forming a contact opening in the inter-level dielectric layer, exposing a portion of a top surface of the substrate adjacent to the spacers; and

forming a contact structure within the contact opening, wherein the spacers and the cap layer separate the contact structure from the patterned gate metal layer enclosed therein.

**15**. The method of claim 14 wherein the gate metal layer has a thickness between 100 and 3,000 Angstroms.

**16**. The method of claim 15 wherein the gate metal layer is made of a material including refractory metal, nitrided metal, or silicide.

**17**. The method of claim 16 wherein the gate metal layer is made of a material including W, Al, AlCu, Cu, Ti, $TiSi_2$, Co, $CoSi_2$, Ni, NiSi, TiN, TiW, or TaN.

**18**. The method of claim 14 wherein the cap layer has a thickness between 50 and 3,000 Angstroms.

**19**. The method of claim 14 wherein depositing a cap layer further comprises:

forming a first cap sublayer atop the gate metal layer; and

forming a second cap sub-layer atop the first cap sub-layer.